

Description

MOSFET With Decoupled Halo Before Extension

BACKGROUND OF INVENTION

- [0001] The field of the invention is that of MOSFET integrated circuit processing with field effect transistors having short channel widths and also having excellent punchthrough characteristics, and which can be realized with a VLSI manufacturable process.
- [0002] In order to fabricate future complex integrated circuits, the basic building block of integrated circuits, the transistor, must become smaller. Smaller metal oxide semiconductor (MOS) transistors are formed by decreasing the channel length of the transistor. Future MOS transistors will have channel lengths of less than 30 nm.
- [0003] Those skilled in the art are aware of a number of problems that become more difficult as the channel length decreases, referred to generally as short channel effects.
- [0004] A particular problem in transistor fabrication is the ability to adjust the threshold V_t and also the on-resistance (series resistance) of the transistor. In conventional practice, the two are linked, so that it is not possible to set the values of the two quantities independently.

[0005] Conventionally, the halo implant is performed with the wafer tilted so that the implanted ions penetrate underneath the gate. In practice, this method increases the capacitance of the device when the diffusion of the extension implant is greater than estimated and also affects the series resistance of the device.

[0006] In particular, a problem with manufacturing such small channel devices is that the punchthrough voltage of these transistors decreases to an unacceptable level.

[0007] The punchthrough voltage of a device is the drain voltage that causes the drain depletion region of the device to extend into the source depletion region. When this occurs the transistor conducts regardless the gate voltage. This eliminates the ability of the transistor to act as a switch, i.e. to switch "on" and "off". MOS transistors of less than 400 nm gate length cannot be fabricated without adjusting to some degree the process recipe to raise the punchthrough voltage of the device.

[0008] Presently the main technique for adjusting the punchthrough voltage and threshold voltage of short channel MOSFET transistors is the halo implant, in which a second implant of the same polarity of the transistor body is made to increase the dopant concentration at the edge of the source and drain and thereby reduce the depletion region. These implants are often made with the wafer oriented at a large tilt with respect to the implanting ions. This implant forms higher concentration P type regions (using an NFET as an example unless otherwise stated) under the gate to prevent bulk punchthrough. This implant is generated

by tilting and rotating the wafer as the implant occurs. The dosage is small enough compared with the dose in the source and drain that they are not affected. The gate acts to block the halo dose from reaching the bulk of the transistor body and confines it to the edge of the body in a small region near the low-doped (LDD) region of the source and drain.

[0009] Halo transistors exhibit several undesirable features. First, the P implants do not surround the entire drain. This requires wells to be deeper to prevent punchthrough leading to a reduction in packing densities. Second, the doping uniformity is dependent on the placement, shape, and layout of the fabricated transistor, since the implanted ions will be blocked by neighboring structures. As dimensions shrink, the aspect ratio of the gap between neighboring devices increases and the degree of blocking the implant also increases. Additionally, the halo technique requires very specialized and expensive equipment which increase the cost of applying the method.

[0010] Thus, what is needed is a reliable submicron transistor which exhibits excellent punchthrough characteristics without sacrificing other device performance characteristics and which can be fabricated with a VLSI manufacturable process.

SUMMARY OF INVENTION

[0011] The invention relates to a method of forming a FET with a halo implant that does not use an angled implant.

[0012] A feature of the invention is the use of the ledges on an inverse-T gate electrode to provide the alignment of a self-aligned halo implant.

[0013] Another feature of the invention is the separation of the deep source/drain (S/D) implant from the halo implant and from the S/D extension implant.

[0014] Yet another feature of the invention is a method of forming an inverse-T gate electrode by etching the gate structure laterally while the ledge area is protected, thereby carving out the ledges from the gate electrode structure.

[0015] Yet another feature of the invention is the formation of an inverse-T gate electrode by a damascene technique in which the electrode is deposited in an aperture in a temporary layer.

BRIEF DESCRIPTION OF DRAWINGS

[0016] Figure 1 shows an initial step in forming an inverse-T gate electrode.

[0017] Figure 2 shows an intermediate step in forming an inverse-T gate electrode.

[0018] Figure 3 shows the result of the etching step in forming an inverse-T gate electrode.

[0019] Figure 4 shows the resulting inverse-T gate electrode.

[0020] Figure 5 the result of a preliminary step of implanting the halo area in the inventive method.

[0021] Figure 6 the result of implanting the deep S/D area in the inventive method.

[0022] Figure 7 the result of implanting the shallow extension implant area in the inventive method.

[0023] Figure 8 shows an initial step in an alternative method of forming an inverse-T gate electrode.

[0024] Figure 9 shows the result of an intermediate step of forming the vertical sidewalls in the damascene aperture in the alternative method of forming an inverse-T gate electrode.

[0025] Figure 10 shows the result of another intermediate step of removing the temporary layer that supported forming the vertical sidewalls in the alternative method of forming an inverse-T gate electrode.

[0026] Figure 11 shows the result of the alternative method.

DETAILED DESCRIPTION

[0027] Figure 5 illustrates a step in a process according to the invention. At the center of the Figure, an inverse-T gate electrode 36 has been formed by any convenient method, such as those discussed below. Electrode 36 has a set of ledges 34 that project to the side by a ledge distance. Unless otherwise indicated, a reference to the gate will include the ledges. In the example, adapted for the 30 nm node, gate 36 has a length of 30 nm and ledges 34 extend by 5 nm to 30 nm, preferably 10 nm out from electrode 36. Ledges 34 have a nominal thickness of 10 nm. Illustratively, the ledges 34 are formed over a transistor axis

extending in the plane of the paper and the sides of the gate before and behind the paper do not have ledges. Other variations having ledges on all four sides of the gate are possible.

[0028] Composite electrode 36 rests on a gate dielectric 32, illustratively thermal oxide. The Figure shows the result of applying a halo implant to form halo 44. In the example shown, the transistor is an N-FET having a body 12 that is P-type and the halo is also P. Those skilled in the art will be aware of conventional magnitudes applying to the P body and to the P halo and will readily be able to adapt the invention to PFETs. The halo implant has been applied by a vertical implant, avoiding the well known problems associated with angled implants. Since the inner portion of the self-aligned halo implant has passed through the ledges 34, the ions have lost energy and consequently, the ions closer in to the gate penetrate into the body 12 to a lesser degree. The depth of the halo in the shallower area will be referred to as the halo depth.

[0029] On the right and left of the Figure, isolating members 20 have been formed by etching a trench and filling it with dielectric, e.g. oxide (SiO_2). Also on the extreme edges of the Figure, a photoresist mask 82 has had an aperture formed in it that blocks the implant in other regions where it is not desired. The substrate 10 in which the transistor is being formed may be bulk or SOI.

[0030] Figure 6 shows the result of the next stage, in which a set of temporary disposable spacers 45 have been formed by a conventional technique of depositing a conformal oxide layer and then directionally etching the

horizontal portions of the layer. The thickness of the layer is set such that the sidewalls extend horizontally past the ledges by some margin. A conventional source/drain (S/D) implant 46 has been formed to a greater depth than the halo implant. The S/D has an upper portion 42 where the dopant concentration of the S/D has been reduced by the effect of the halo and a lower portion 46 that is N+. The magnitude of the S/D implant dose is chosen relative to the halo implant so that the resistivity of the S/D is reduced to a desired amount. One of the benefits of the present invention is that the various implants are decoupled, so that the resistivity of the transistor in the on state can be set without being adversely affected by the halo. The spacers 45 are stripped at any convenient time, e. g. before the following step. Also, the thermal step of activating the S/D and halo implants is performed before the extension implant that will follow.

[0031]

Figure 7 illustrates the result of forming the final implant, which forms the extension of the S/D, referred to as the extension implant. It can be seen in Figures 6 and 7 that the horizontal extent of the N+ implant was set by the width of the spacers, leaving an area between the N+ implant of the S/D and the ledge that is P-type. The extension implant counterdopes the silicon in that area, resulting in a final dopant concentration suitable for a LDD structure as is known to those skilled in the art. The energy of the extension implant is selected such that it does not penetrate the leaving the halo implant beneath the ledges unaffected. The extension implant, since it is shallow, is activated by a

rapid thermal anneal (RTA) step, such as nominally 900Å°C for 5 seconds.

[0032] It is an advantageous feature of the invention that the halo and the extension are decoupled. They are set by different implant steps and are physically separated. Thus, the VT of the transistor, as affected by the halo implant, is not affected by the extension implant, which affects the on-resistance of the transistor and the hot-electron effects.

[0033] Figure 8 illustrates a step in forming an inverse-T transistor that may be used with the previous method. A substrate 10 has STI isolation members 20 bounding a body area as before. A gate electrode layer 32, illustratively thermal oxide, has been grown and a ledge layer 34, illustratively polysilicon, that will form the ledges of the inverted T structure has been deposited. A nitride layer 84 has been put down to a depth suitable for the gate electrode, e.g. 10 nm to 100 nm, preferably 50 nm and an aperture 56 has been formed in the nitride layer, extending down to the ledge layer using conventional photolithography and dry etching.

[0034] In Figure 9, vertical oxide spacers 52 have been formed according to the technique taught in U.S. Patent 6,190,961. The thickness of these spacers will define the extent of the projection of the ledges in the final transistor. Such a vertical spacer is preferred, but not necessary, and a conventional spacer process may also be used. After spacer 52 have been formed, the remaining portion of the aperture is filled with poly by chemical vapor deposition (CVD) and chemical mechanical polish

(CMP).

[0035] The nitride damascene layer is stripped by selective etching such as a hot phosphoric acid wet etch, leaving the structure shown in Figure 10 having a central electrode 58 bracketed by the vertical spacers.

[0036] A selective anisotropic directional etch trims off the ledges to the width of the spacers 52, after which the spacers are stripped, leaving the final structure shown in Figure 11. The S/D and halo may then be formed according to the previous example or with an alternative technique.

[0037] Another technique for forming an inverse-T electrode transistor is illustrated in Figures 1 - 4.

[0038] Figure 1 shows an initial structure in which a substrate 10 has had a gate oxide 32 grown on it and a poly layer has been put down and patterned to form a first gate structure 36'.

[0039] A HDP oxide layer 22 having a thickness suitable for the thickness of the transistor ledges has been put down on the horizontal surfaces. If the deposition step leaves some oxide adhering to the vertical edges of the gate, that may be cleaned up in an isotropic etch. The result is shown in Figure 2.

[0040] A wet etch or other isotropic etch removes poly from gate 36' to an amount indicated by dotted lines 24, leaving a ledge 34 on the bottom where the horizontal etching action has been blocked by the blocking layer 22.

[0041] The final result is shown in Figure 4, with the final gate 36 having the ledges 34 defined by the horizontal etching step.

[0042] While the invention has been described in terms of a single preferred embodiment, those skilled in the art will recognize that the invention can be practiced in various versions within the spirit and scope of the following claims.